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In this post we introduce the gm/ID (transconductance efficiency) methodology used in analog circuit design to determine MOS W/L (width over channel length) ratios for designing differential amplifiers, operational transconductance amplifiers, etc. We will

provide setup test circuits to retrieve the relevant specs from SPICE simulators such as Cadence Virtuoso and Advanced Design System (ADS), use...

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A Basic Introduction to the gm /ID -Based Design Methodology 0.1 Abstract This article introduces the reader to the gm /ID -based design methodology, which is a way to help CMOS analog circuit designers link physical transistor parameters to small signal models.

A Basic Introduction to the gm ID-Based Design

Based Methodology for the Design of CMOS Analog Circuits and Its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA F. Silveira, D. Flandre, P.G.A. Jespers IEEE JOURNAL OF SOLID STATE CIRCUITS, VOL. 31, NO. 9, SEPTEMBER 1996 p. 1314 ... BWRC, Dec 12, 2008. P.G.A. Jespers First paper. 13 BWRC, Dec 12, 2008. P.G.A. Jespers Outline Sizing... • the Intrinsic Gain Stage (I.G.S ...

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The gm/ID ratio is a measure of the efficiency to translate current (hence power) into transconductance; i.e., the greater the gm/ID value, the greater the transconductance we obtain at a constant current value. Therefore, the gm/ID ratio is 0018-9200/96\$05.00 0 1996 IEEE Authorized licensed use limited to: Universidad de la Republica ...

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CMOS stage using symbolic analysis and gm/ID methodology", IEEE Journal of Solid-State Circuits (Special Issue on 22nd ESSCIRC conference), 32 (1997) 1006-1012. z

Silveira F., Flandre D., Jespers P.G.A. A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-ion- insulator micropower OTA. IEEE Journal of Solid State Circuits. Vol. 31 ...

Design of MOS Amplifiers Using gm/ID Methodology

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